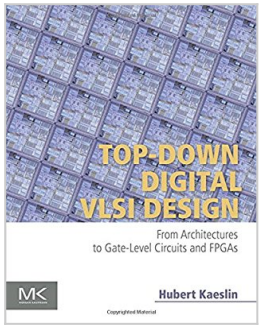

Top-Down Digital VLSI Design: From Architectures to Gate-Level Circuits and FPGAs

By Hubert Kaeslin

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Top-Down VLSI Design: From Architectures to Gate-Level Circuits and FPGAs represents a unique approach to learning digital design. Developed from more than 20 years teaching circuit design, Doctor Kaeslin's approach follows the natural VLSI design flow and makes circuit design accessible for professionals with a background in systems engineering or digital signal processing. It begins with hardware architecture and promotes a system-level view, first considering the type of intended application and letting that guide your design choices.

Doctor Kaeslin presents modern considerations for handling circuit complexity, throughput, and energy efficiency while preserving functionality. The book focuses on application-specific integrated circuits (ASICs), which along with FPGAs are increasingly used to develop products with applications in telecommunications, IT security, biomedical, automotive, and computer vision industries. Topics include field-programmable logic, algorithms, verification, modeling hardware, synchronous clocking, and more.

- Demonstrates a top-down approach to digital VLSI design.
- Provides a systematic overview of architecture optimization techniques.
- Features a chapter on field-programmable logic devices, their technologies and architectures.
- Includes checklists, hints, and warnings for various design situations.
- Emphasizes design flows that do not overlook important action items and which include alternative options when planning the development of microelectronic circuits.

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Editorial Review

From the Back Cover

There can be no information technology without microelectronics. *Top-Down Digital VLSI Design: From Architectures to Gate-Level Circuits and FPGAs* covers the design of microchips for applications as diverse as telecommunication, data security, real-time video processing, and more. Focusing on front-end design, this text explains how a suitable circuit architecture can be devised for a given set of signal or data processing algorithms. The architecture is modeled with the aid of a hardware description language, which allows for the verification of the model code and the synthesizing of the code into a gate-level netlist. In addition to "mask-programmed" ASICs (Application-Specific Integrated Circuit), this book also addresses the emergence and importance of field-programmable logic devices, which now share much of the front-end design flow with classic ASICs.

About the Author
Since 1989, Hubert Kaeslin has headed the Micro-electronics Design Center of ETH Zurich, which taped out more than 300 circuit designs under his supervision over the past 23 years, both for research and educational purposes. He has written more than 75 scientific papers and his professional interests extend to digital signal processing, IT security, graph theory, and visual formalisms. Dr. Kaeslin is a Senior Member of IEEE and has been awarded the title of professor by ETH in 2010.

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